ABSTRACT

A semiconductor package 11 which has a plurality of connection terminals 14 to be connected to a board and a plurality of test terminals 15, which usually do not need to be connected to the board and are for performance test by the maker, on a joint surface 12 thereof to the board. Placed in the semiconductor package are a predetermined-pitch area 16 where the connection terminals 14 are arranged at predetermined pitches in a lattice and a narrow-pitch area 17 where the test terminals 15 are arranged at pitches narrower than the predetermined pitches in a lattice.